

### **REMARKS**

Applicant has carefully reviewed and considered the Office Action mailed on September 23, 2004, and the references cited therewith. This amendment cancels no claims, amends no claims, and adds no new claims. As a result, claims 1-26 are now pending in this application.

#### **Double Patenting Rejection**

Claims 9-14, 16, and 18-26 were rejected under the judicially created doctrine of double patenting over claims 1, 3-6, 9, and 11-18 respectively of U.S. Patent No. 6,779,013.

Applicant will revisit the issue and, if appropriate, submit a terminal disclaimer to obviate this rejection when at least some independent claims have been found otherwise allowable.

#### **§112 Rejection of the Claims**

Claims 2-7, 15, and 26 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses the rejections of claims 2-7, 15, and 26.

With regards to claim 2, the Office Action alleges that "an exponent weight of one" is unclear whether the least significant bit of the exponent starts at bit 0<sup>th</sup> or the exponent has a base of 2. Applicant respectfully disagrees regarding the indefiniteness of the quoted passage. Applicant respectfully submits that the claim language in question, when analyzed in light of the content of the application disclosure, is not indefinite. The application disclosure, at page 7, line 3, provides that, "The exponent of the product,  $E_p$ , is an eight bit number with a least significant bit weight equal to one. For example, an  $E_p$  field of 00000011 has a value of three, because the least significant bit has a weight of one, and the next more significant bit has a weight of two. For the purposes of this description, this exponent format is termed 'base 2,' and the product is said to be in base 2." The application disclosure further discusses base 2 number representations at numerous points, including page 10, line 29 through page 11, line 10. Applicant respectfully

submits that the rejection of claim 2 has been overcome, and that claim 2 is in condition for allowance.

With regards to claims 3, 4, 6, 15, and 26, the Office Action alleges that "an exponent weight of thirty two" is unclear whether the least significant bit of the exponent starts at bit 4<sup>th</sup> or the exponent has a base of 32. Applicant respectfully disagrees regarding the indefiniteness of the quoted passage. Applicant respectfully submits that the claim language in question, when analyzed in light of the content of the application disclosure, is not indefinite. The application disclosure, at page 7, line 7, provides that "Floating point conversion unit 220 converts the product from base 2 to a different base. For example, exponent path 312 is an exponent conversion unit that sets the least significant five bits of the exponent field to zero, and *truncates the exponent field to three bits*, leaving the least significant bit of the exponent of the converted product,  $E_{cp}$ , *with a weight of 32*," (emphasis added) and further, at page 9, line 24, "Figure 5 shows a floating point conversion unit. Floating point conversion unit 220 receives eight bit exponent field of the product,  $E_p[7:0]$ , where  $E_p[7]$  is the most significant bit, and  $E_p[0]$  is the least significant bit. The exponent of the converted product,  $E_{cp}$ , is created by removing the least significant five bits from the exponent field.  *$E_{cp}$  has a least significant bit equal to  $E_p[5]$ , which has a weight of thirty-two*." (emphasis added) Applicant respectfully submits that the rejections of claims 3, 4, 6, 15, and 26 have been overcome, and that claims 3, 4, 6, 15, and 26 are in condition for allowance.

With regards to claim 6, the Office Action states "'three bit exponent field having a least significant bit weight of thirty-two' is indefinite because in order for a bit to have a weight of thirty-two, that bit must be at least at fifth position." Applicant respectfully disagrees with this statement, and respectfully submits that the claim language in question, when analyzed in light of the content of the application disclosure, is not indefinite. The application disclosure, at page 7, line 13, provides that "For example, an  $E_{cp}$  field of 011 has a value of 96, because the least significant bit has a weight of 32, and the next more significant bit has a weight of 64. For the purposes of this description, this exponent format is termed 'base 32,' and the converted product is said to be in base 32," and further, at page 11, line 11 "Exponent 724 is equal to the most

significant three bits of exponent 714. The least significant bit of exponent 724 has a 'weight' of thirty-two." Therefore, Applicant objects to the Examiner disregarding this limitation, and respectfully submits that the objection to claim 6, including the limitation "three bit exponent field having a least significant bit weight of thirty-two," has been overcome, and that claim 6 is in condition for allowance.

Claims 5 and 7 were rejected as being dependent on the rejected base claims 4 and 6 respectively. Applicant respectfully submits that the objections to the rejected base claims 4 and 6 have been overcome, and therefore claims 5 and 7 are in condition for allowance.

#### §102 Rejection of the Claims

Claims 1-2, 8-9, 13-14, 18, and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wyland *et al.* (U.S. 6,205,462). Applicant does not admit that Wyland *et al.* is prior art and reserves the right, as provided for under 37 C.F.R. § 1.131, to "swear behind" Wyland *et al.* However, Applicant also urges that the claims distinguish the reference, and therefore respectfully traverses the rejections of claims 1-2, 8-9, 13-14, 18, and 20.

Claim 1 recites "a floating point conversion unit to convert the product from the first exponent weight to a converted product with *a second exponent weight*." (emphasis added) In contrast, Wyland *et al.* at column 4, lines 20-27, states "Exponent sum 141 generated by adder 140 is the sum of two exponents E1 and E2 and hence represents the exponent of mantissa product 143. With the sum of exponents and final fixed point data format known, the necessary number of shifting places for the product of mantissas can be calculated and, therefore, shifter 144 can be designed accordingly to implement this shifting." Hence, Wyland *et al.* teaches an "exponent sum generated by adder 140," but fails to teach "a second exponent weight" for the exponent, and therefore fails to teach each of the elements of claim 1.

Similarly, claim 9 recites "an exponent conversion unit coupled to the output of the exponent summer, *to convert the product exponent to a second weight*." (emphasis added) Further, claim 18 recites "converting the product to have a *different least significant bit weight exponent field*." (emphasis added) For reasons analogous to those stated above, Applicant submits that Wyland *et al.* fails to recite "to convert the product exponent to a second weight," and fails to recite, "a different least significant bit weight exponent field," as recited in claims 9

and 18 respectively, and so fails to teach each of the elements of claims 9 and 18. Thus, the Office Action fails to state a *prima facie* case of anticipation with respect to claims 1, 9, and 18.

Claims 2 and 8 depend from claim 1; claims 13 and 14 depend from claim 9; and claim 20 depends from claim 18. For reasons analogous to those stated above and elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of anticipation with respect to claims 2, 8, 13-14, and 20. For the above and other reasons, Applicant urges that claims meet all the statutory requirements, and ought to be allowed. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 2, 8, 13-14, and 20.

#### §103 Rejection of the Claims

Claims 12, 16-17, and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wyland *et al.* (U.S.6,205,462) in view of Dibrino *et al.* (U.S. 6,542,915). Applicant does not admit that either Wyland *et al.* or Dibrino *et al.* is prior art and reserves the right to "swear behind" Wyland *et al.* and Dibrino *et al.* as provided for under 37 C.F.R. § 1.131. However, Applicant also asserts that the rejected claims distinguish any combination of the references that might be proper under 35 U.S.C. § 103, and so respectfully traverses the rejections of claims 12, 16-17, and 19.

The Office Action must provide specific, objective evidence of record for a finding of a teaching, suggestion, or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action, in an attempt to meet this requirement, on page 5 states, "Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the product mantissa accumulator comprising four-to-two compressors in carry-save format as seen in Dibrino *et al.*'s invention into Wyland *et al.*'s invention because it would enable to reduce the circuitry and increase the system performance in multiplying mantissa." This statement does not meet the standard established by *In re Sang Su Lee* in that the Office Action must "explain the reasoning by which the evidence is deemed to support such a finding." For example, the Office Action fails to point out in the record where the

addition of the product mantissa accumulator of Dibrino *et al.* would "reduce the circuitry" of Wyland *et al.* Further, the abstract of Dibrino *et al.* states, "Presented is a 'high-order' Leading Zero Anticipator or LZA circuit," yet the Office Action fails to indicate whether this function is performed, or even required, by Wyland *et al.* Thus, by failing to meet the standard of *In re* Sang Su Lee, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 12, 16-17, and 19. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 12, 16-17, and 19.

Even assuming *arguendo* that Wyland *et al.* and Dibrino *et al.* are not improperly combined, the Office Action still fails to state a *prima facie* case of obviousness with respect to claims 12, 16-17, and 19.

Claims 12 and 16-17 depend from claim 9, and therefore include all the elements of claim 9. Claim 19 depends from claim 18, and therefore includes all the elements of claim 18. As noted above, claim 9 recites, "an exponent conversion unit coupled to the output of the exponent summer, to convert the product exponent to a second weight," and claim 18 recites, "converting the product to have a different least significant bit weight exponent field." For reasons analogous to those stated above, Applicant respectfully submits that Wyland *et al.* fails to teach or suggest these elements. Further, Dibrino *et al.* at column 2, lines 62-64, states, "FIG. 1 illustrates a typical floating-point pipeline. This diagram shows the 'Mantissa' dataflow only (the exponent dataflow logic is not shown)," and at column 6, lines 63-66, "FIG. 8 represents pipeline stage 2 of the floating-point pipeline of FIG. 1 with the prior art two-input LZA block 101 replaced by the new 'high-order' LZA 801, with N=5 (A five-input LZA)," and at column 7, lines 4-5, "Elements 804, 807, 808, 809, 810 operate similarly to blocks 104, 107, 108, 109, 110." Hence, Dibrino *et al.* also fails to teach or suggest each of the elements as recited in claims 9 and 18. Applicant respectfully submits that neither Wyland *et al.* nor Dibrino *et al.*, either alone or in combination, teach or suggest each of the elements of claims 9 and 18, so the Office Action fails to state a *prima facie* case of obviousness with respect to claims 12, 16-17, and 19. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 12, 16-17, and 19.

*Allowable Subject Matter*

Claims 10-11 and 21-25 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant acknowledges the Examiner's indication of allowability of claims 10-11 and 21-25 if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has not amended claims 10-11 and 21-25 to place them in independent form at this time. Pursuant to arguments presented above, Applicant respectfully submits that these claims are in condition for allowance.

Claims 3-5, 7, 15, and 26 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112 set forth in the Office Action.

Applicant acknowledges the Examiner's indication of allowability of claims 3-5, 7, 15, and 26 if rewritten to overcome the rejection(s) under 35 U.S.C. § 112 set forth in the Office Action. Applicant has not rewritten claims 3-5, 7, 15, and 26 at this time. Pursuant to arguments presented above, Applicant respectfully submits that the rejections under 35 U.S.C. § 112 have been overcome, and therefore these claims are in condition for allowance.

*Documents Cited but Not Relied Upon for this Office Action*

Applicant has reviewed the cited references that were not applied to the claims, and agrees that the claims distinguish over them in a patentable manner.

*Information Disclosure Statement*

Applicant notes that an incompletely-initialed copy of a 1449 form was returned with the Office Action. Specifically, the Examiner failed to initial the U.S. Patent Documents (US-5,764,089; US-5,898,330; US-5,900,759) listed on the first 1449 form included with the Office Action. A copy of the returned 1449 form is enclosed. Applicant requests that the Examiner complete the consideration of the Information Disclosure Statement filed with the present application and return a completely-initialed copy of the 1449 form.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111  
Serial Number: 09/873,557  
Filing Date: June 4, 2001  
Title: FLOATING POINT MULTIPLY ACCUMULATOR  
Assignee: Intel Corporation

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Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6971) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

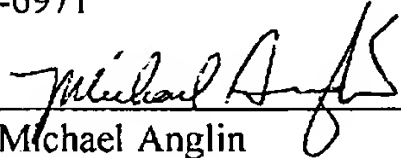
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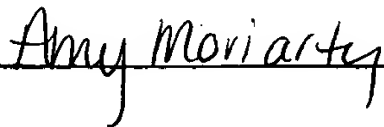
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By

  
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15<sup>th</sup> day of December, 2004.

Name



Signature

